Abstract—In this paper, a VLSI architecture of turbo decoder employing an efficient stopping criterion is proposed. The new stopping criterion algorithm is based on Hard Decision Aided (HDA) stopping criterion algorithm, using phase estimation method to reduce iterations also improve turbo decoding efficiency. In high SNR environment, the proposed algorithm requires less iterations without losing error correction ability compared to traditional stop criteria algorithms. In addition, it can save power consumption due to decoding termination within single iteration. As for low SNR environment, we can stop iteration immediately when it detects the received data can not be decoded. The proposed algorithm can stop the turbo decoder earlier than traditional methods in both high SNR and low SNR environment. Finally, for verifying the proposed algorithm, a turbo decoder using new phase estimation is designed with TSMC 0.18μm 1P6M process, the chip size is 1530μm × 1504μm and working frequency is 48MHz.

Index Terms—Turbo decoder, stopping criterion, phase estimation, hard decision.

I. INTRODUCTION

Turbo coding has an excellent error correction capability by utilizing an iterative algorithm, which allows its coding gain near to Shannon-limit [1]. Nowadays, some of channel coding standards, such as 3GPP/3GPP2, IEEE802.16d/802.16e, global system mobile (GSM), and code division multiple access (CDMA) have chosen it as their optional channel decoder.

Turbo decoder is consisted of two necessary Soft-In Soft-Out (SISO) decoders. These two SISO decoders perform an iterative algorithm and exchange information from one to the other. The operation acts among two SISO decoders named iteration, which decides them major decoding latency and power consumption of turbo decoder. Here, the procedure combines with sequential and interleaved phase decoding called an iteration. Normally, a specified number of maximum iteration is set for terminating decoding. A considerable issue is not every iteration can increasingly improve the decoding performance. Therefore, some researches choose log likelihood ratio (LLR) or Extrinsic estimation, hard decision.

The well-known two earlier stop iteration algorithms are Sign Change Ratio (SCR) algorithm and Hard Decision Aided (HDA) algorithm [3]. SCR algorithm needsto consider the threshold value very carefully because the chosen value affects the coding gain significantly. The criterion of HDA algorithm is to compare the hard decision bits between two iterations and to terminate iteration when the comparison remains the same result. A modification of HDA algorithm called HDA-DHDD algorithm [4] is proposed in 2005. It stops the iteration when DHDD satisfy the threshold value. Generally speaking, many earlier stop iteration algorithms terminate their decoding after completing a single iteration. In this paper, a new stopping iteration algorithm based on phase criterion is proposed. Thus, it can give the ability to reduce decoding latency and save power consumption.

This paper is organized as follows. Section II introduces the turbo encoder and decoder. In Section III, we describe a new stop criterion algorithm based on phase estimation that can improve decoding efficiency. Section IV illustrates the architecture of proposed turbo decoder. Conclusions are given in Section V.

II. TURBO ENCODER AND DECODER

A. Turbo Encoder

The turbo encoder is composed of two parallel concatenated recursive systematic convolutional (RSC) encoders [5]. The first element encoder receives uncoded (systematic) data bits \( u_k \) in order and outputs a set of parity bits \( x_1^s \). The second element encoder receives a permutation of the uncoded data bits from a block interleaver and outputs a second set of parity bits \( x_2^s \). The systematic bits and the two set of parity bits are sent to the channel. It is shown in Fig. 1.

![Fig. 1. Block diagram of turbo encoder.](image)

B. Turbo Decoder

The turbo decoder is made up of two elementary SISO decoders. Each SISO decoder has three input ports: \( y_1 \) is the received systematic bit from the channel, \( y_2 \) is the received parity bit from the channel, and \( L_i \) is called priori LLR. Two output ports: \( L_v \) is the extrinsic information bit, \( L_r \) is the LLR. The turbo decoder diagram is shown in Fig. 2[6]. In initial setting, the \( L_{2-deint}^r \) set to zero. When SISO1 receives the...
III. PHASE ESTIMATION HARD DECISION STOP CRITERION

A. Concept of Proposed Stop Criterion

Traditional stop criteria use iteration as computing cycle to check its stop condition [8-11]. In this section, a phase estimation stopping criterion based on HDA algorithm is proposed. The proposed algorithm is called Phase Estimation Hard Decision (PEHD) stopping criterion. It operates the stop criterion after one phase operation is completed. We call the operation of decoding in SISO1 as sequential phase and in SISO2 as interleaver phase, the diagram is shown in Fig. 3. PEHD algorithm not only reduces total numbers of iteration in high SNR, but also can detect the damaged degree of received data and terminate immediately in low SNR.

First, PEHD algorithm compares $L_1(\hat{u})$ with $L_2(\hat{u})$ when every phase operation completed in stop criterion operation circuit as Fig. 3 shows. When $\text{sign}(L(\hat{u}))$ is exact, that implies $L_1(\hat{u})$ and $L_2(\hat{u})$ are constant values even doing further iteration decoding. In other words, $L_1(\hat{u})$ could be exact values before $L_2(\hat{u})$ when turbo decoding is successful.

As Fig. 3 depicts, $L_1(\hat{u})$ is generated in sequential phase but $L_2(\hat{u})$ is generated in interleavered phase. Therefore, it has to confirm that the data order of $L_1(\hat{u})$ and $L_2(\hat{u})$ must be the same before to do stop criterion operation. When error is free, the relationship between $L_1(\hat{u})$ and $L_2(\hat{u})$ are listed below:

\[ L_1(\hat{u}) = L_2(\pi^{-1}(\hat{u})) \]  
\[ L_2(\hat{u}) = L_1(\pi(\hat{u})) \]

where $\pi$ is an interleave function, $\pi^{-1}$ is a de-interleave function.

In terms of above descriptions, when $L_2(\hat{u})$ is compared with $L_2(\hat{u})$ in sequential phase, $L_2(\hat{u})$ has to be deinterleaved to confirm their data order are the same first. Similarly, $L_1(\hat{u})$ has to be interleaved before $L_2(\hat{u})$ compared with it in interleaver phase.

B. Decoding Convergence in High SNR

Fig. 2. Diagram of traditional turbo decoder.

\[ \text{Fig. 3. Structure diagram of proposed turbo decoder.} \]

\[ \text{Fig. 4. Relationship diagram of sign}(L_1(\hat{u})), \text{sign}(L_2(\hat{u})) \text{and number of phase operation in SNR 3dB.} \]

Turbo decoder usually can correct all errors of received data successfully when it is in high SNR. In this situation, the relationship between $\text{sign}(L_1(\hat{u}))$, $\text{sign}(L_2(\hat{u}))$ and phase operation times is shown in Fig. 4. Where $\text{sign}(L_1(\hat{u}))$ and $\text{sign}(L_2(\hat{u}))$ mean sign bits of $L_1(\hat{u})$ and $L_2(\hat{u})$. The simulation frame size is 10000 and SNR is 3dB. EVT1 to EVT9 are evaluation times 1 to 9.

Equal bits of $\text{sign}(L_1(\hat{u}))$ and $\text{sign}(L_2(\hat{u}))$ are getting higher and higher when times of phase operation are increasing.

Therefore, the equal bits between $\text{sign}(L_1(\hat{u}))$ and $\text{sign}(L_2(\hat{u}))$ are proportional to operation times of phase when turbo decoder in high SNR situation.

C. Decoding Divergence in Low SNR

On the contrast, turbo decoder can’t correct all errors of received data successfully when it in low SNR. The relationship between $\text{sign}(L_1(\hat{u})), \text{sign}(L_2(\hat{u}))$ and number of phase operation in low SNR is shown in Fig. 5. Where its frame size 10000 and SNR is 0 dB.

\[ \text{Fig. 5. Relationship diagram of sign}(L_1(\hat{u})), \text{sign}(L_2(\hat{u})) \text{and number of phase operation in SNR 0dB.} \]
Fig. 5. Relationship diagram of $\text{sign}(L_{1}(\hat{u}))$, $\text{sign}(L_{2}(\hat{u}))$ and number of phase operation in SNR 0dB.

Fig. 5 demonstrates equal bits relationship between $\text{sign}(L_{1}(\hat{u}))$ and $\text{sign}(L_{2}(\hat{u}))$. These random even operation times of phase are increasing. In other words, the relationship between $\text{sign}(L_{1}(\hat{u}))$ and $\text{sign}(L_{2}(\hat{u}))$ is irregular when turbo decoder is in low SNR situation.

D. New Stop Criterion

In order to satisfy decoding convergence and divergence conditions, the stopping criteria of proposed new algorithm are described as below:

1) If $\text{sign}(L_{1}(\hat{u}))$ of $i$th phase operation equals to $\text{sign}(L_{2}(\hat{u}))$ of $(i-1)$th phase operation totally in sequential phase, or $\text{sign}(L_{2}(\hat{u}))$ of $i$th phase operation equals to $\text{sign}(L_{1}(\hat{u}))$ of $(i-1)$th phase operation totally in interleaved phase, then the proposed algorithm stops turbo decoder.

2) If the equivalent values between $\text{sign}(L_{1}(\hat{u}))$ and $\text{sign}(L_{2}(\hat{u}))$ of $i$th phase operation are larger than $(i+1)$th phase operation, then proposed algorithm stops turbo decoder.

In high SNR situation, turbo decoder usually can correct errors successfully and stop criteria conditions of four algorithms could be satisfied. Due to traditional stop criteria compute their stop criterion condition after one iterative decoding is completed, so they need at least two iterations to verify their stop criterion. It increases the decoding time and power consumption of turbo decoder.

The PEHD algorithm computes its stop criterion after every one phase operation completed as illustrated in Fig. 6. That means it can compute its stop criterion twice in one iteration. Therefore, it only needs one iterative operation in best condition.

IV. ARCHITECTURE OF PEHD TURBO DECODER

The proposed algorithm is compared with other three stop criteria, HDA, SCR, and HDA-DHDD. The error correction performance of stop criteria is simulated on same turbo decoder platform and it is shown in Fig. 7.

Based on Fig. 7, it indicates the BER performance of PEHD algorithm is almost the same as other three stopping criteria. VLSI architecture of turbo decoder adopting PEHD algorithm is shown in Fig. 8, it is composed of SISO, received data buffers, interleaver and deinterleaver data ROM, extrinsic data buffers and PEHD stopping criterion circuit. PEHD algorithm needs a memory that can be read first and written last on same clock edge to store previous $\text{sign}(L_{1}(\hat{u}))$ or $\text{sign}(L_{2}(\hat{u}))$. These stopping criteria are summarized in Table I. The PEHD algorithm has the earlier stop iteration function in both high SNR and low SNR environment. Moreover, it has less number of iterations and the total decoding timethat can save more power consumption compared to other algorithms.

Fig. 6. Average numbers of iteration diagram of HDA, SCR, HDA-DHDD and proposed algorithm.

Fig. 7. BER performance of HDA, SCR, HDA-DHDD and proposed algorithm.

Fig. 8. Turbo decoder architecture with proposed algorithm.

Fig. 9. Chip layout diagram with proposed stop criterion algorithm.
Finally, this new phase estimation hard decision stop criterion turbo decoder has been designed with TSMC 0.18μm 1P6M process. Table II shows the specifications of chip. The decoder chip size is 1530μm × 1504μm, working frequency is 48MHz. The chip layout is shown as Fig. 9.

<table>
<thead>
<tr>
<th>Algorithm</th>
<th>Stop Criterion</th>
<th>Minimum Iteration</th>
<th>Operation unit of stop criterion</th>
<th>Stop Criterion Demand</th>
</tr>
</thead>
<tbody>
<tr>
<td>HDA</td>
<td>Δsign(L_{i}(\hat{u})) = 0</td>
<td>2</td>
<td>Iteration</td>
<td>Yes</td>
</tr>
<tr>
<td>HDA-DHDD</td>
<td>DHDD &lt; (0.01)N</td>
<td>2</td>
<td>Iteration</td>
<td>No</td>
</tr>
<tr>
<td>SCR</td>
<td>C(i) &lt; (0.005)N</td>
<td>2</td>
<td>Iteration</td>
<td>Yes</td>
</tr>
<tr>
<td>Proposed</td>
<td>(a) When sign(L_{i+1}(\hat{u})), equals sign(L_{i}(\hat{u})), totally. (b) When i-th equivalent value is larger than (i+1)-th, between sign(L_{i}(\hat{u})), and sign(L_{i+1}(\hat{u})).</td>
<td>1</td>
<td>Phase</td>
<td>Yes</td>
</tr>
</tbody>
</table>

TABLE II: SPECIFICATIONS OF PROPOSED TURBO DECODER

<table>
<thead>
<tr>
<th>Process</th>
<th>TSMC 0.18μm 1P6M</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interleaver type</td>
<td>S-Random</td>
</tr>
<tr>
<td>Interleaver size</td>
<td>1024-bit</td>
</tr>
<tr>
<td>Constraint length</td>
<td>3</td>
</tr>
<tr>
<td>Generator Polynomial</td>
<td>(7, 5)</td>
</tr>
<tr>
<td>Code rate</td>
<td>1/3</td>
</tr>
<tr>
<td>Decoding algorithm</td>
<td>SW-Log-MAP</td>
</tr>
<tr>
<td>Sliding window size</td>
<td>16-bit</td>
</tr>
<tr>
<td>Total cells</td>
<td>18786</td>
</tr>
<tr>
<td>Operation frequency</td>
<td>48MHz</td>
</tr>
<tr>
<td>Chip area (include PAD)</td>
<td>1530μm x 1504μm</td>
</tr>
</tbody>
</table>

V. CONCLUSIONS

A new Phase Estimation Hard Decision stopping iteration criterion is proposed. It can stop the turbo decoder earlier than traditional methods in both high SNR and low SNR environment. In best condition, it only needs one iteration for turbo decoding. Thus, the proposed PEHD method can give a low-power and low-latency solution for chip integration.

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REFERENCES


Wen-Ta Lee was born in Taipei, Taiwan, R.O.C., in 1962. He received the B.S. and M.S. degrees in Department of Electrical Engineering from National Cheng Kung University, in 1985 and 1989, respectively. He also received the Ph.D. degree in Department of Electrical Engineering from National Taiwan University, in 1995. He is now an Associate Professor in the Department of Electronic Engineering, National Taipei University of Technology. His research interests are in the areas of VLSI architectures for digital communications, coding theory and signal processing.

Yao-Chang Chang was born in Taoyuan, Taiwan, R.O.C., in 1977. He received the M.S. degree in the Institute of Computer and Communication from National Taiwan University of Technology in 2009. He is currently a Senior Design Engineer at Navoton Technology Company, Ltd., Hsinchu Science Park, Taiwan, since 2009. His research interests are the fields of digital signal processing, digital communications and ARM architecture.